FIG. 1

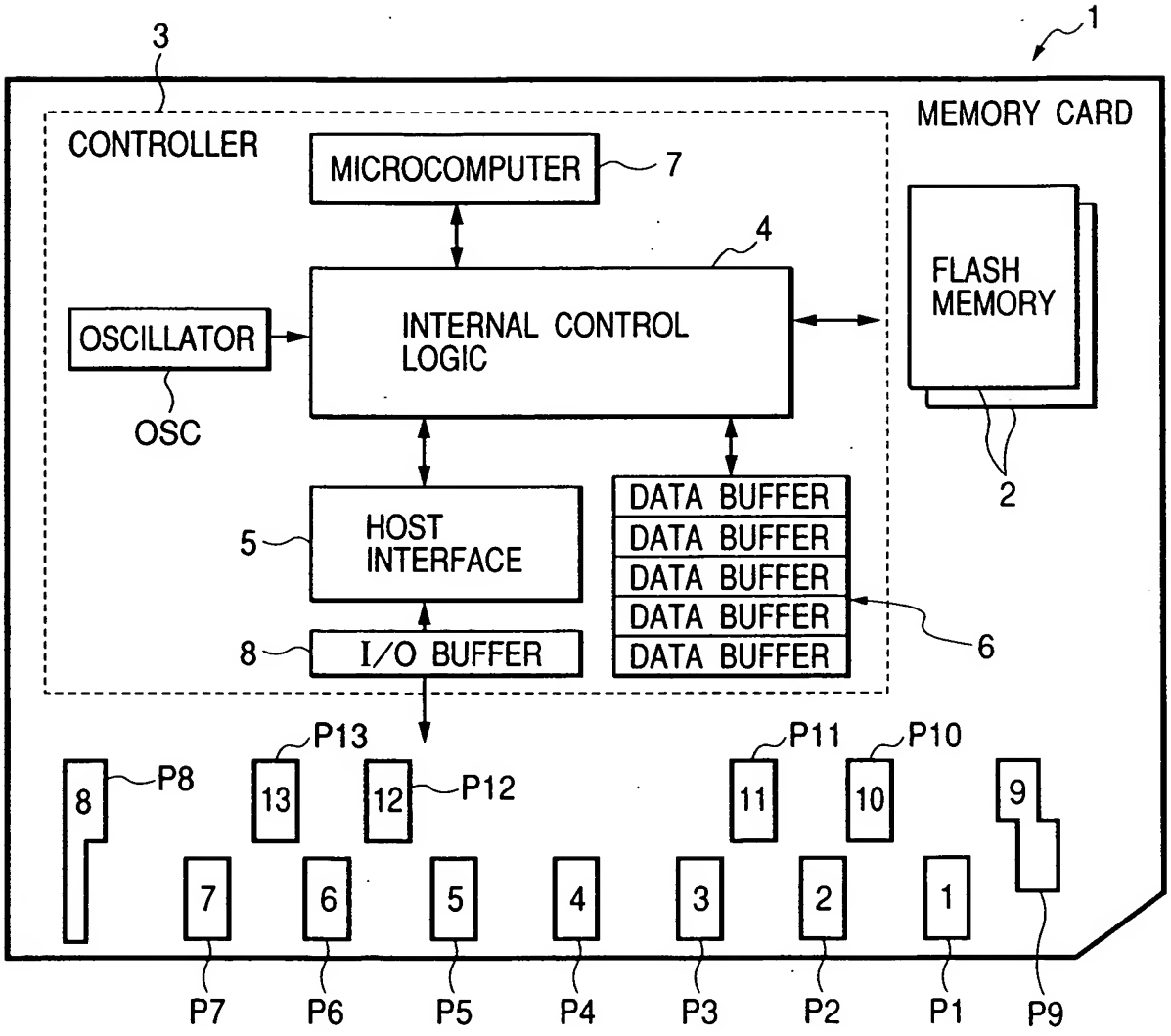

1
3
MEMORY CARD
CONTROLLER
MICROCOMPUTER
7
4
FLASH MEMORY
OSCILLATOR
INTERNAL CONTROL LOGIC
OSC
2
5
HOST INTERFACE
DATA BUFFER
DATA BUFFER
DATA BUFFER
DATA BUFFER
DATA BUFFER
6
8
I/O BUFFER
P13
P11
P10
8
P8
13
12
P12
11
10
9
7
6
5
4
3
2
1
P7
P6
P5
P4
P3
P2
P1
P9

FIG. 2

PIN NO.	NAME OF PIN	I/O	CONTENTS
1	DAT3	I/O	DATA BUS BIT [3]
2	CMD	I/O	COMMAND
3	VSS1	-	GROUND
4	VCC	-	POWER SUPPLY
5	CLK	I	CLOCK
6	VSS2	-	GROUND
7	DAT0	I/O	DATA BUS BIT [0]
8	DAT1	I/O	DATA BUS BIT [1]
9	DAT2	I/O	DATA BUS BIT [2]
10	DAT4	I/O	DATA BUS BIT [4]
11	DAT5	I/O	DATA BUS BIT [5]
12	DAT6	I/O	DATA BUS BIT [6]
13	DAT7	I/O	DATA BUS BIT [7]

FIG. 3

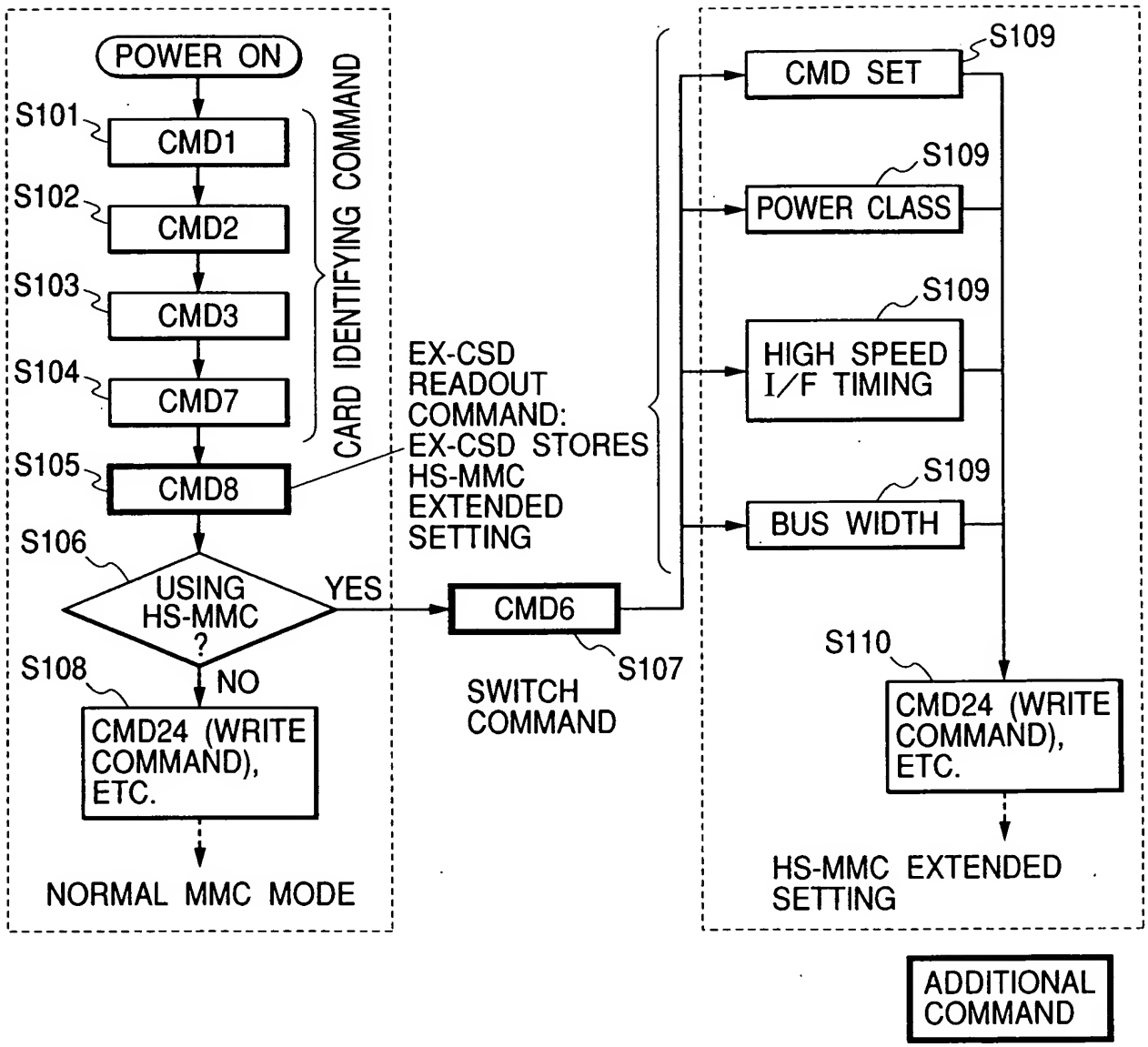

POWER ON
S101
CMD1
S102
CMD2
S103
CMD3
S104
CMD7
CARD IDENTIFYING COMMAND
S105
CMD8
EX-CSD READOUT COMMAND: EX-CSD STORES HS-MMC EXTENDED SETTING
S106
USING HS-MMC ?
YES
NO
S108
CMD24 (WRITE COMMAND), ETC.
NORMAL MMC MODE
CMD6
S107
SWITCH COMMAND
S109
CMD SET
S109
POWER CLASS
S109
HIGH SPEED I/F TIMING
S109
BUS WIDTH
S110
CMD24 (WRITE COMMAND), ETC.
HS-MMC EXTENDED SETTING
ADDITIONAL COMMAND

FIG. 4

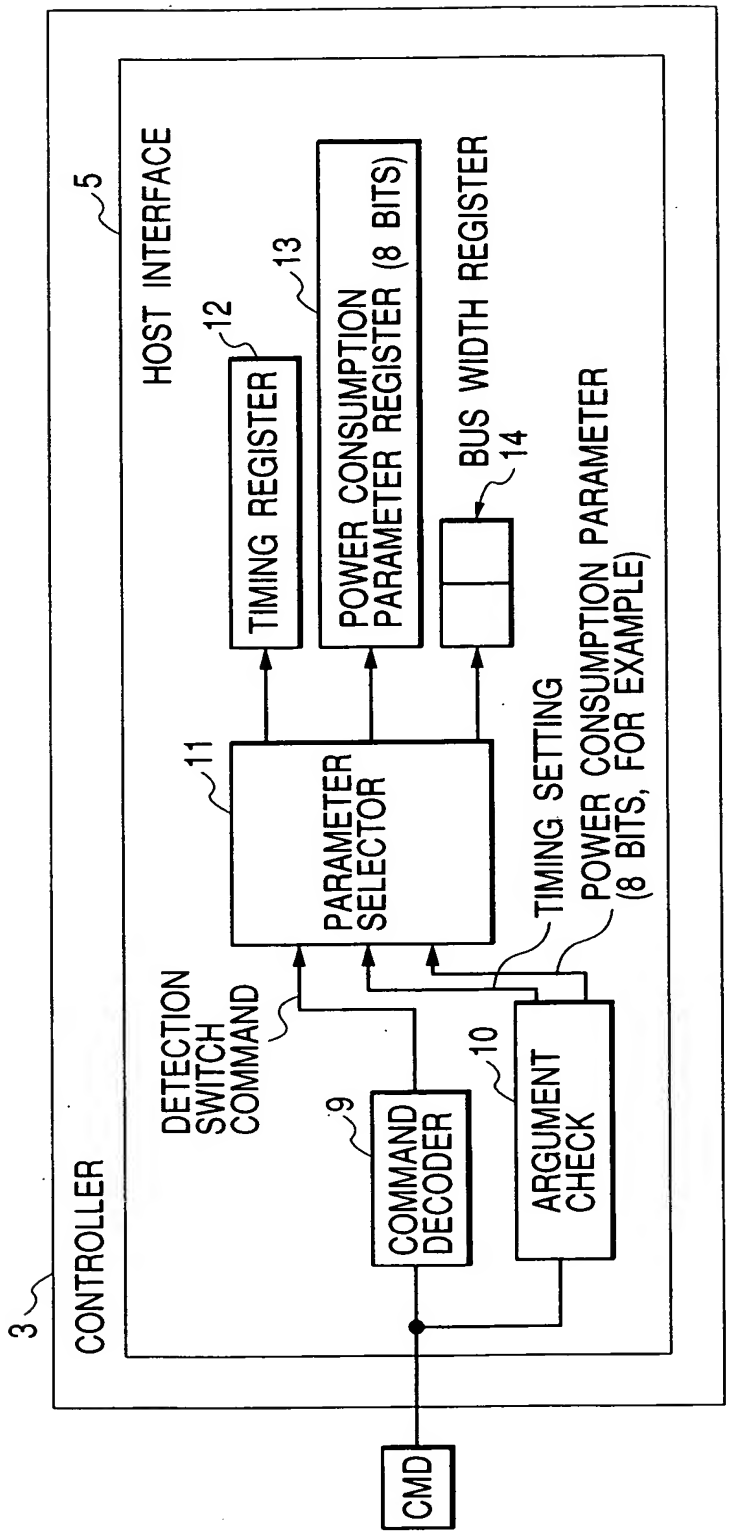

3
CONTROLLER
5
HOST INTERFACE
12
TIMING REGISTER
13
POWER CONSUMPTION PARAMETER REGISTER (8 BITS)
14
BUS WIDTH REGISTER
11
PARAMETER SELECTOR
DETECTION SWITCH COMMAND
9
COMMAND DECODER
10
ARGUMENT CHECK
TIMING SETTING
POWER CONSUMPTION PARAMETER (8 BITS, FOR EXAMPLE)
CMD

FIG. 5

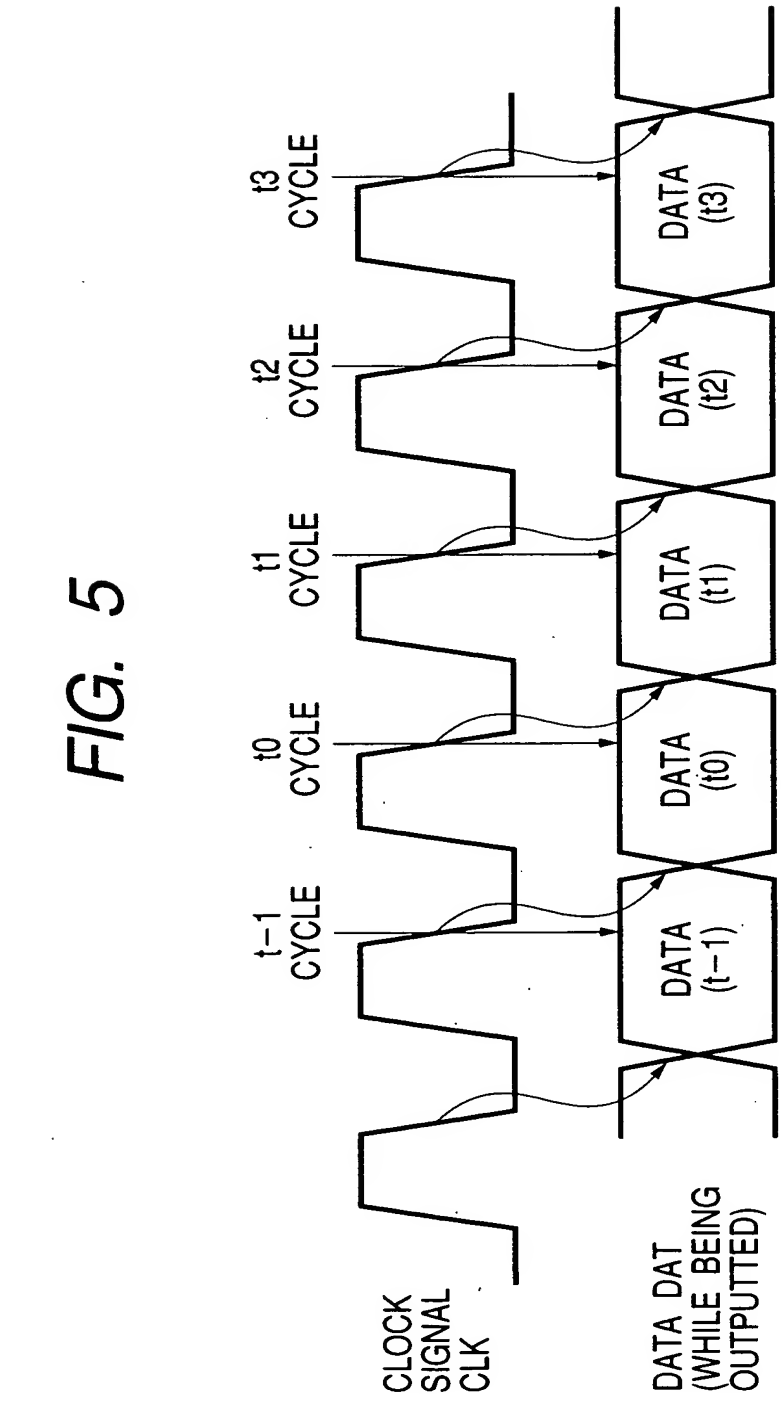

CLOCK SIGNAL CLK
DATA DAT (WHILE BEING OUTPUTTED)
t-1 CYCLE
t0 CYCLE
t1 CYCLE
t2 CYCLE
t3 CYCLE
DATA (t-1)
DATA (t0)
DATA (t1)
DATA (t2)
DATA (t3)

FIG. 6

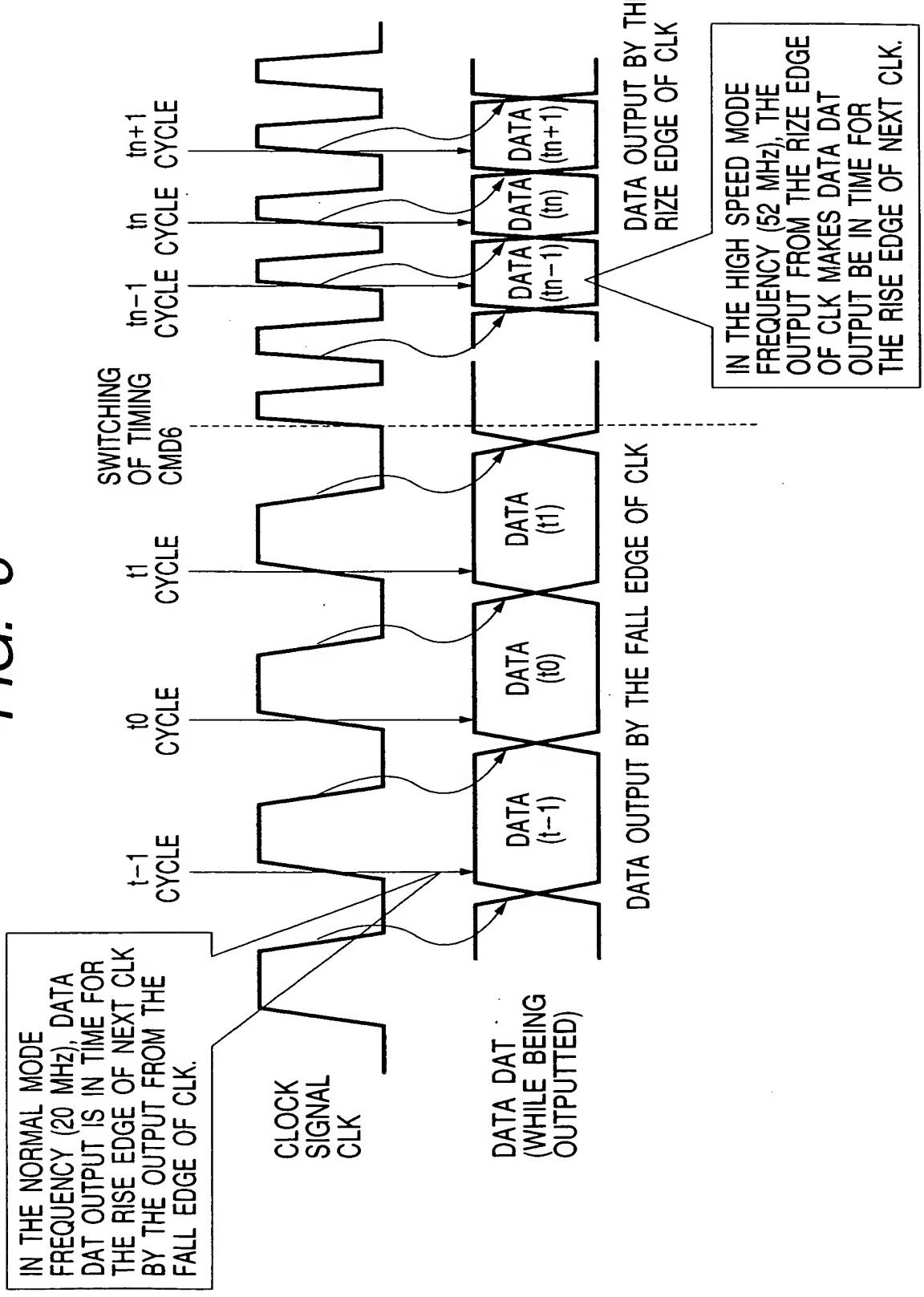

IN THE NORMAL MODE FREQUENCY (20 MHz), DATA DAT OUTPUT IS IN TIME FOR THE RISE EDGE OF NEXT CLK BY THE OUTPUT FROM THE FALL EDGE OF CLK.
t-1 CYCLE
t0 CYCLE
t1 CYCLE
SWITCHING OF TIMING CMD6
tn-1 CYCLE
tn CYCLE
tn+1 CYCLE
CLOCK SIGNAL CLK
DATA DAT (WHILE BEING OUTPUTTED)
DATA (t-1)
DATA (t0)
DATA (t1)
DATA (tn-1)
DATA (tn)
DATA (tn+1)
DATA OUTPUT BY THE FALL EDGE OF CLK
DATA OUTPUT BY THE RIZE EDGE OF CLK
IN THE HIGH SPEED MODE FREQUENCY (52 MHz), THE OUTPUT FROM THE RIZE EDGE OF CLK MAKES DATA DAT OUTPUT BE IN TIME FOR THE RISE EDGE OF NEXT CLK.

FIG. 7

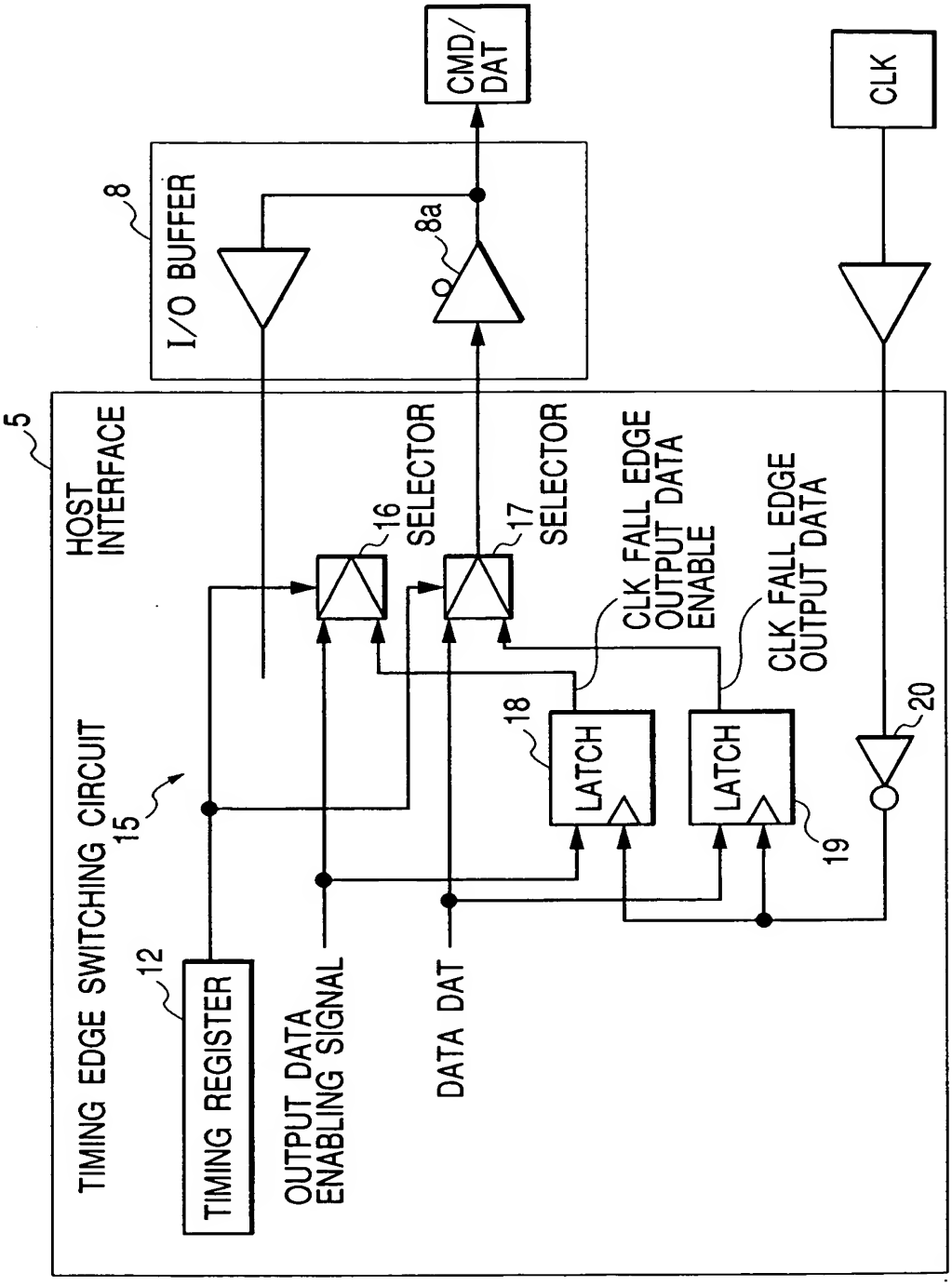

CMD/
DAT
CLK
8
I/O BUFFER
8a
5
HOST
INTERFACE
16
SELECTOR
17
SELECTOR
CLK FALL EDGE
OUTPUT DATA
ENABLE
CLK FALL EDGE
OUTPUT DATA
18
LATCH
LATCH
19
20
TIMING EDGE SWITCHING CIRCUIT
15
12
TIMING REGISTER
OUTPUT DATA
ENABLING SIGNAL
DATA DAT

FIG. 8

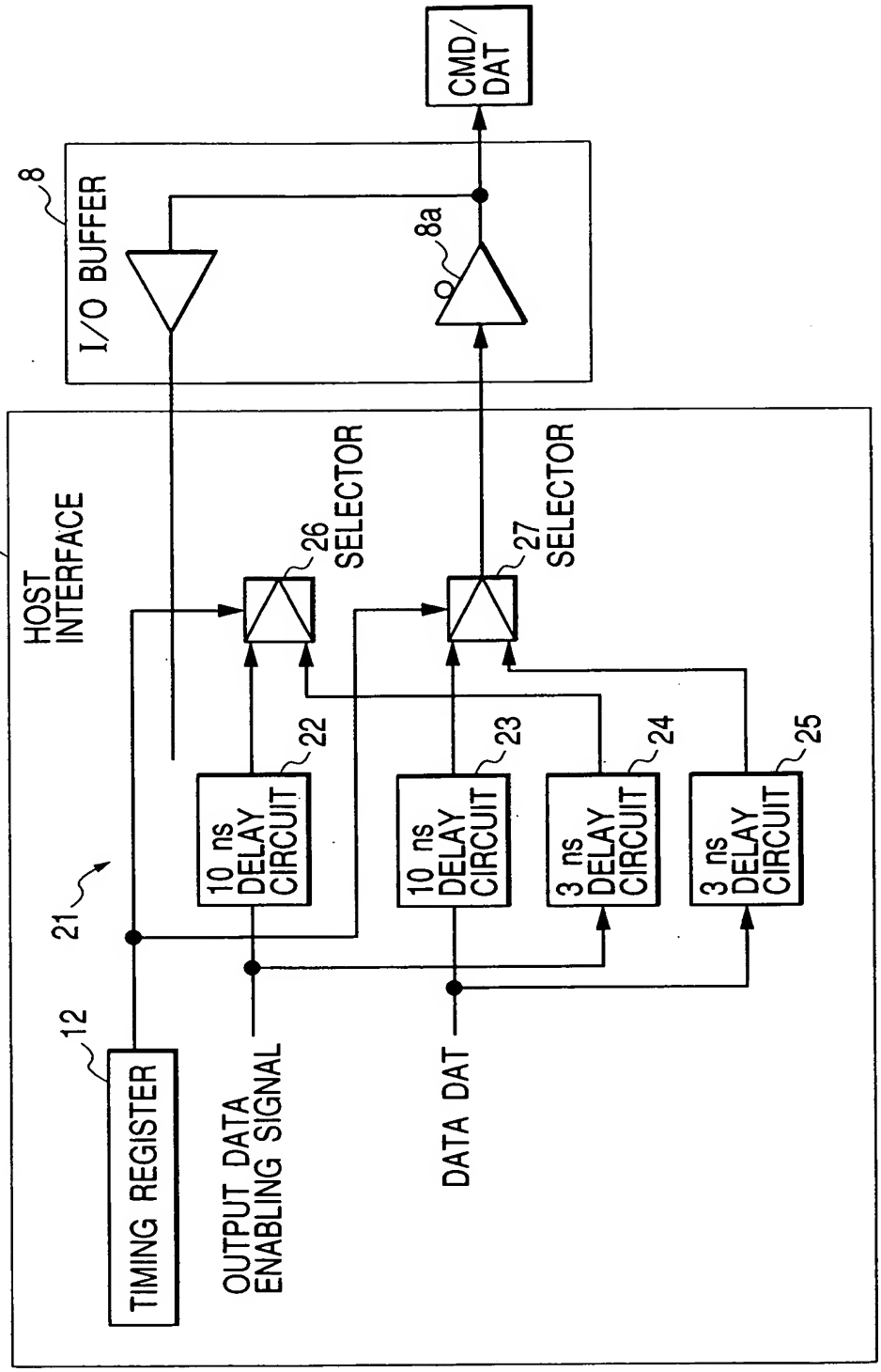

CMD/
DAT
8
I/O BUFFER
8a
5
HOST
INTERFACE
26
SELECTOR
27
SELECTOR
22
23
24
25
10 ns
DELAY
CIRCUIT
10 ns
DELAY
CIRCUIT
3 ns
DELAY
CIRCUIT
3 ns
DELAY
CIRCUIT
21
12
TIMING REGISTER
OUTPUT DATA
ENABLING SIGNAL
DATA DAT

FIG. 9

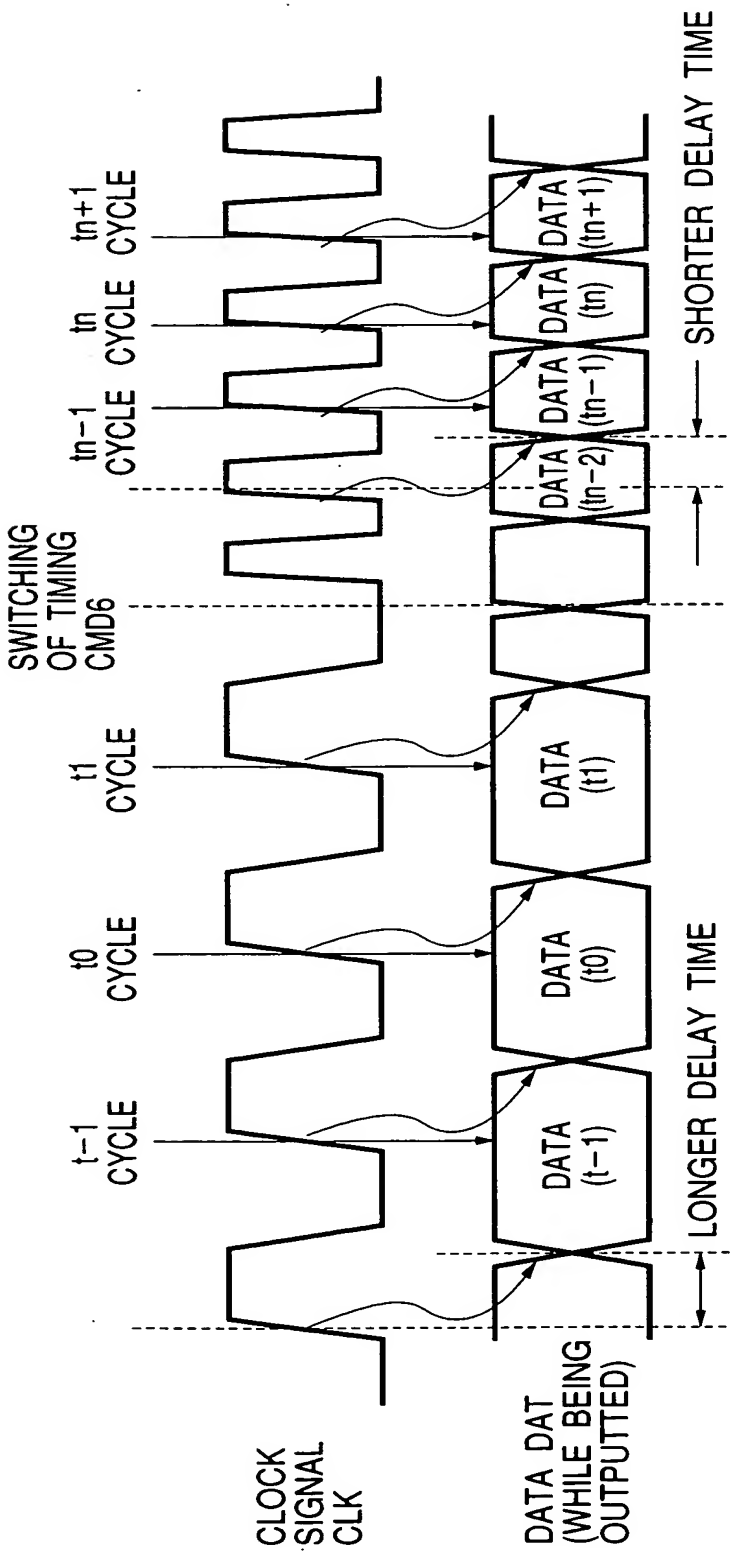

CLOCK SIGNAL CLK
DATA DAT (WHILE BEING OUTPUTTED)
t-1 CYCLE
t0 CYCLE
t1 CYCLE
SWITCHING OF TIMING CMD6
tn-1 CYCLE
tn CYCLE
tn+1 CYCLE
DATA (t-1)
DATA (t0)
DATA (t1)
DATA (tn-2)
DATA (tn-1)
DATA (tn)
DATA (tn+1)
LONGER DELAY TIME
SHORTER DELAY TIME

FIG. 10

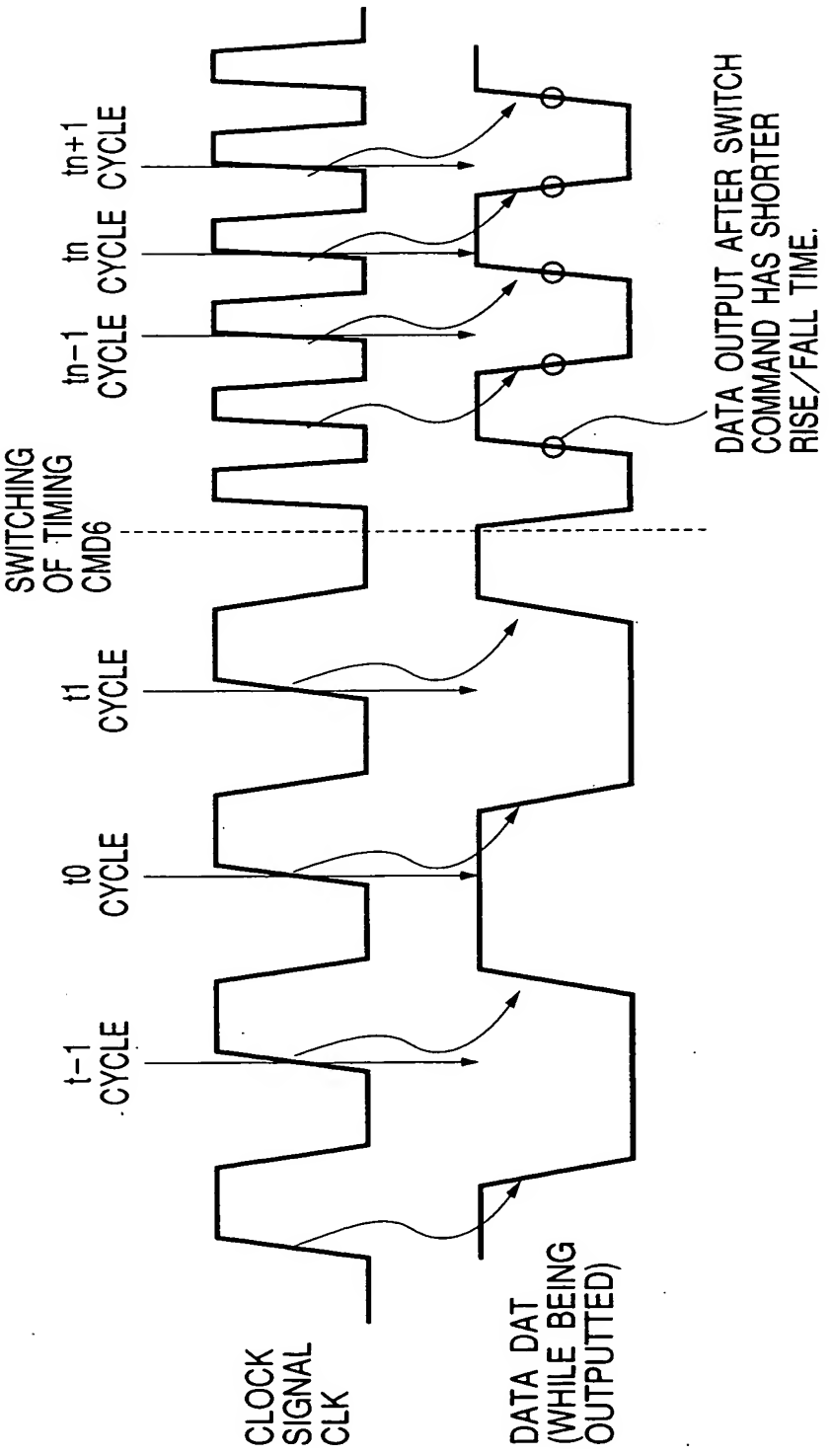

CLOCK SIGNAL CLK
DATA DAT (WHILE BEING OUTPUTTED)
t-1 CYCLE
t0 CYCLE
t1 CYCLE
SWITCHING OF TIMING CMD6
tn-1 CYCLE
tn CYCLE
tn+1 CYCLE
DATA OUTPUT AFTER SWITCH COMMAND HAS SHORTER RISE/FALL TIME.

FIG. 11

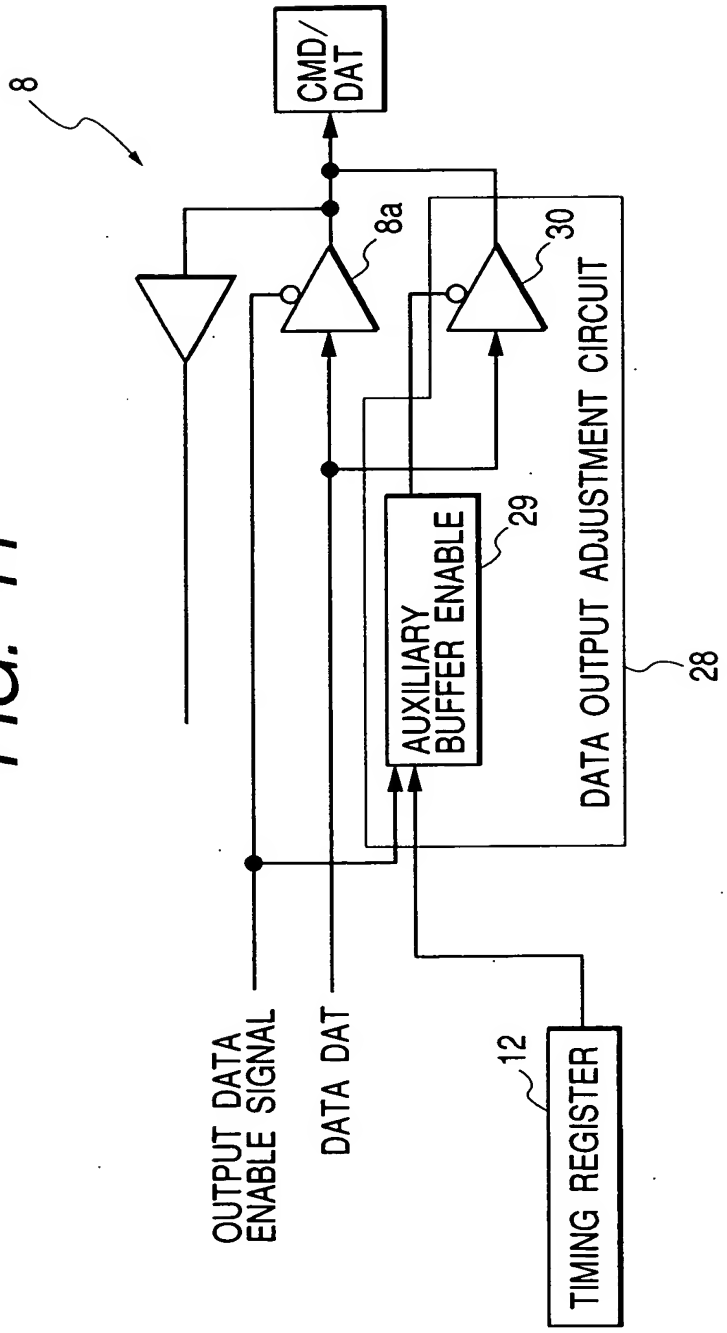

8
CMD/
DAT
8a
30
AUXILIARY
BUFFER ENABLE
29
DATA OUTPUT ADJUSTMENT CIRCUIT
28
OUTPUT DATA
ENABLE SIGNAL
DATA DAT
12
TIMING REGISTER

FIG. 12

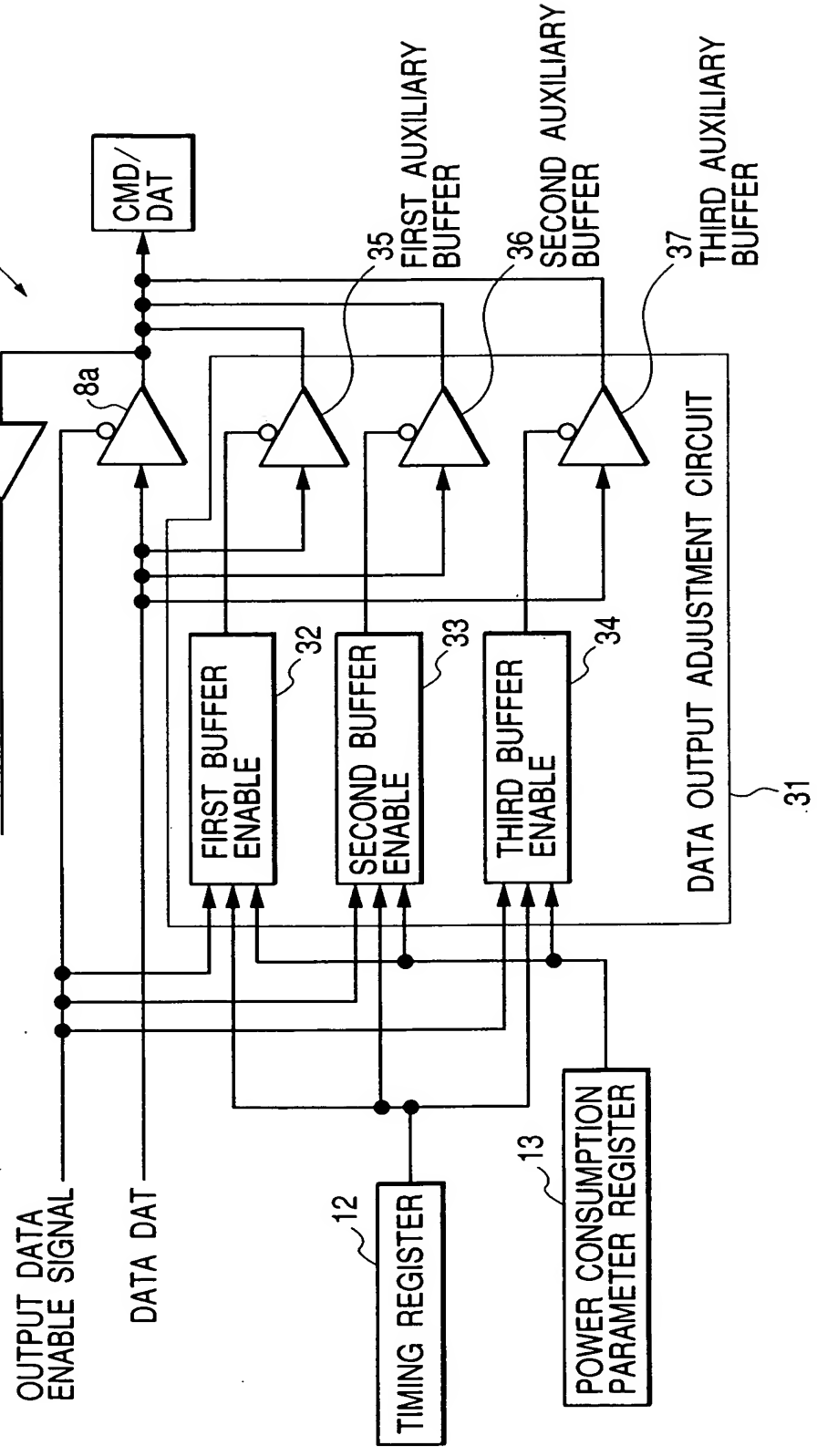

8
CMD/
DAT
8a
35
FIRST AUXILIARY
BUFFER
36
SECOND AUXILIARY
BUFFER
37
THIRD AUXILIARY
BUFFER
FIRST BUFFER
ENABLE
32
SECOND BUFFER
ENABLE
33
THIRD BUFFER
ENABLE
34
DATA OUTPUT ADJUSTMENT CIRCUIT
31
OUTPUT DATA
ENABLE SIGNAL
DATA DAT
12
TIMING REGISTER
13
POWER CONSUMPTION
PARAMETER REGISTER

FIG. 13

TIMING REGISTER	POWER CONSUMPTION	FIRST AUXILIARY BUFFER	SECOND AUXILIARY BUFFER	THIRD AUXILIARY BUFFER
0	DON'T CARE	OFF	OFF	OFF
1	1	ON	OFF	OFF
	2	ON	ON	OFF
	3	ON	ON	ON

FIG. 14

POWER CONSUMPTION PARAMETER REGISTER	SOURCE OSCILLATION FREQUENCY	SYSTEM CLOCK
0 (MAX 100mA)	20MHz	5MHz
1 (MAX 150mA)	20MHz	6.6MHz
2 (MAX 200mA)	20MHz	10MHz
3 (MAX 250mA)	20MHz	20MHz

FIG. 15

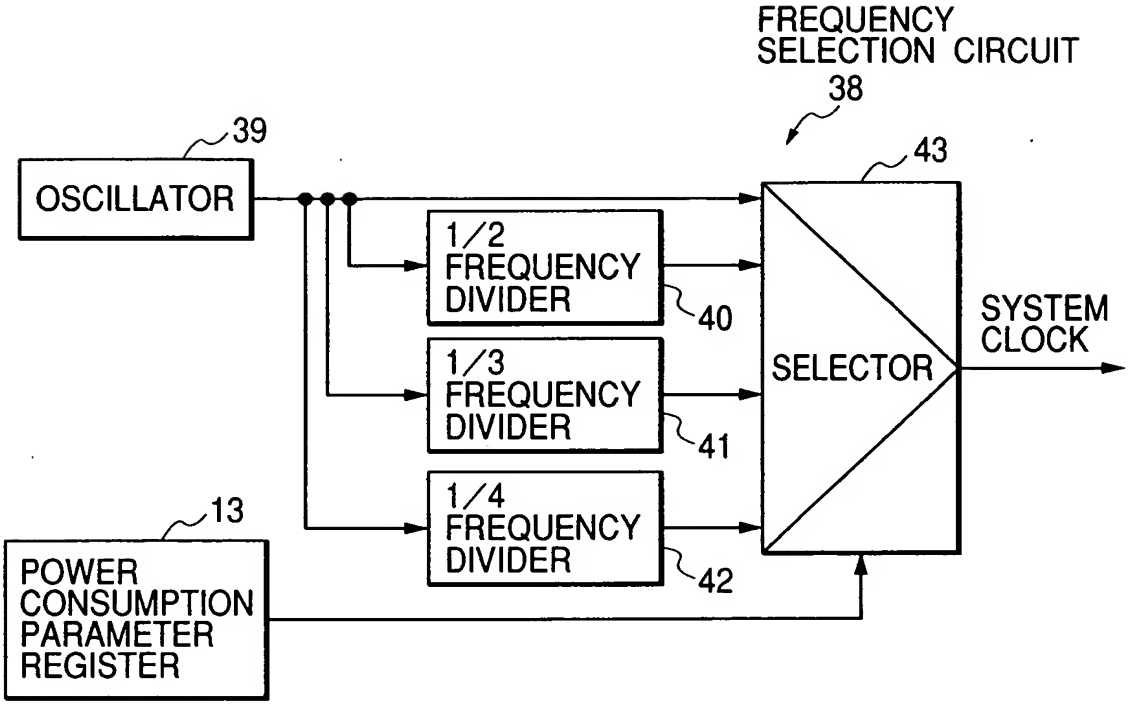


FIG. 16

POWER CONSUMPTION PARAMETER REGISTER	PARALLEL OPERATIONAL NUMBER OF FLASH MEMORY
0 (MAX 100mA)	1
1 (MAX 150mA)	2
2 (MAX 200mA)	3
3 (MAX 250mA)	4

FIG. 17

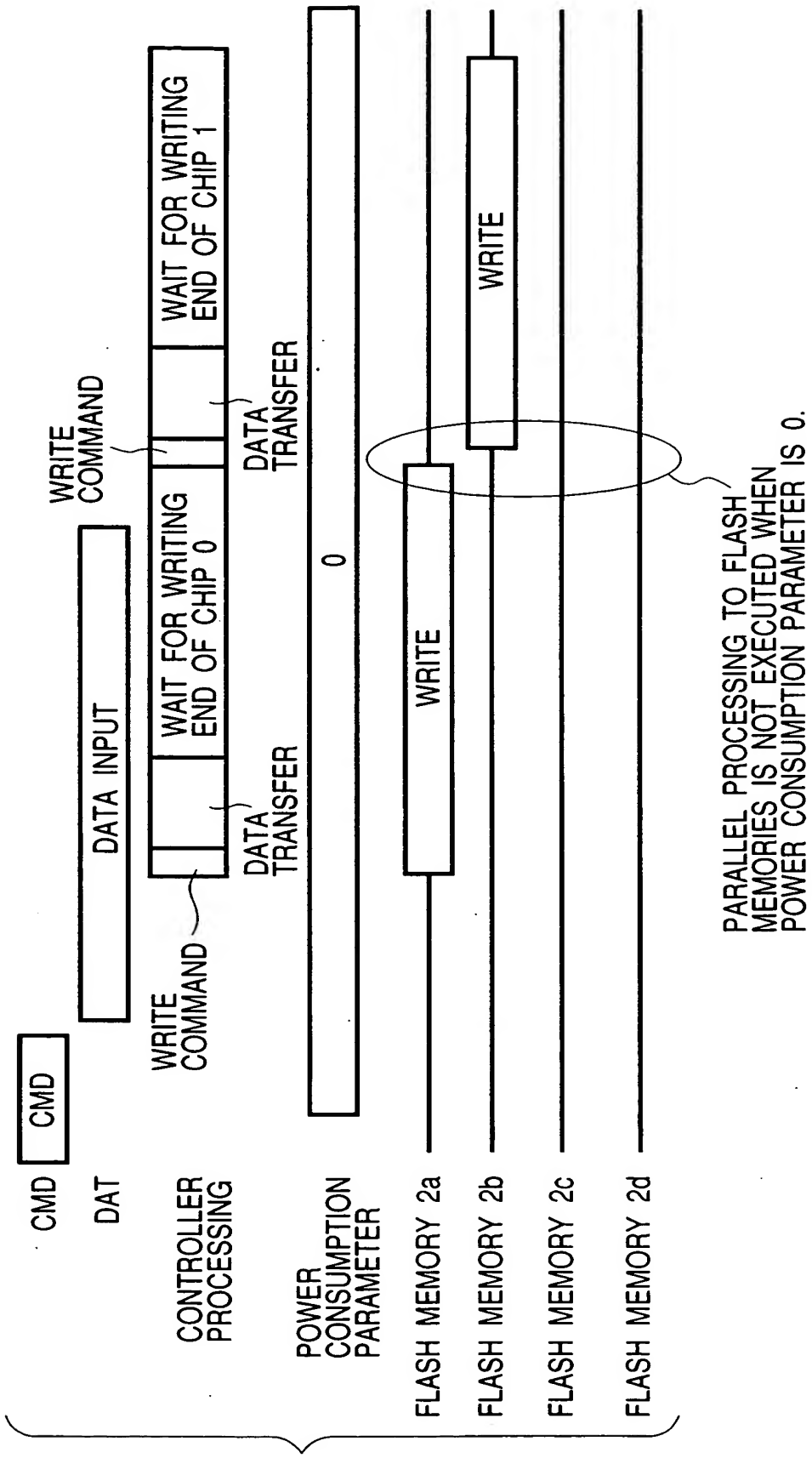

CMD
DAT
CONTROLLER PROCESSING
POWER CONSUMPTION PARAMETER
FLASH MEMORY 2a
FLASH MEMORY 2b
FLASH MEMORY 2c
FLASH MEMORY 2d
CMD
DATA INPUT
WRITE COMMAND
WAIT FOR WRITING END OF CHIP 0
DATA TRANSFER
WRITE COMMAND
WAIT FOR WRITING END OF CHIP 1
DATA TRANSFER
0
WRITE
WRITE
PARALLEL PROCESSING TO FLASH MEMORIES IS NOT EXECUTED WHEN POWER CONSUMPTION PARAMETER IS 0.

FIG. 18

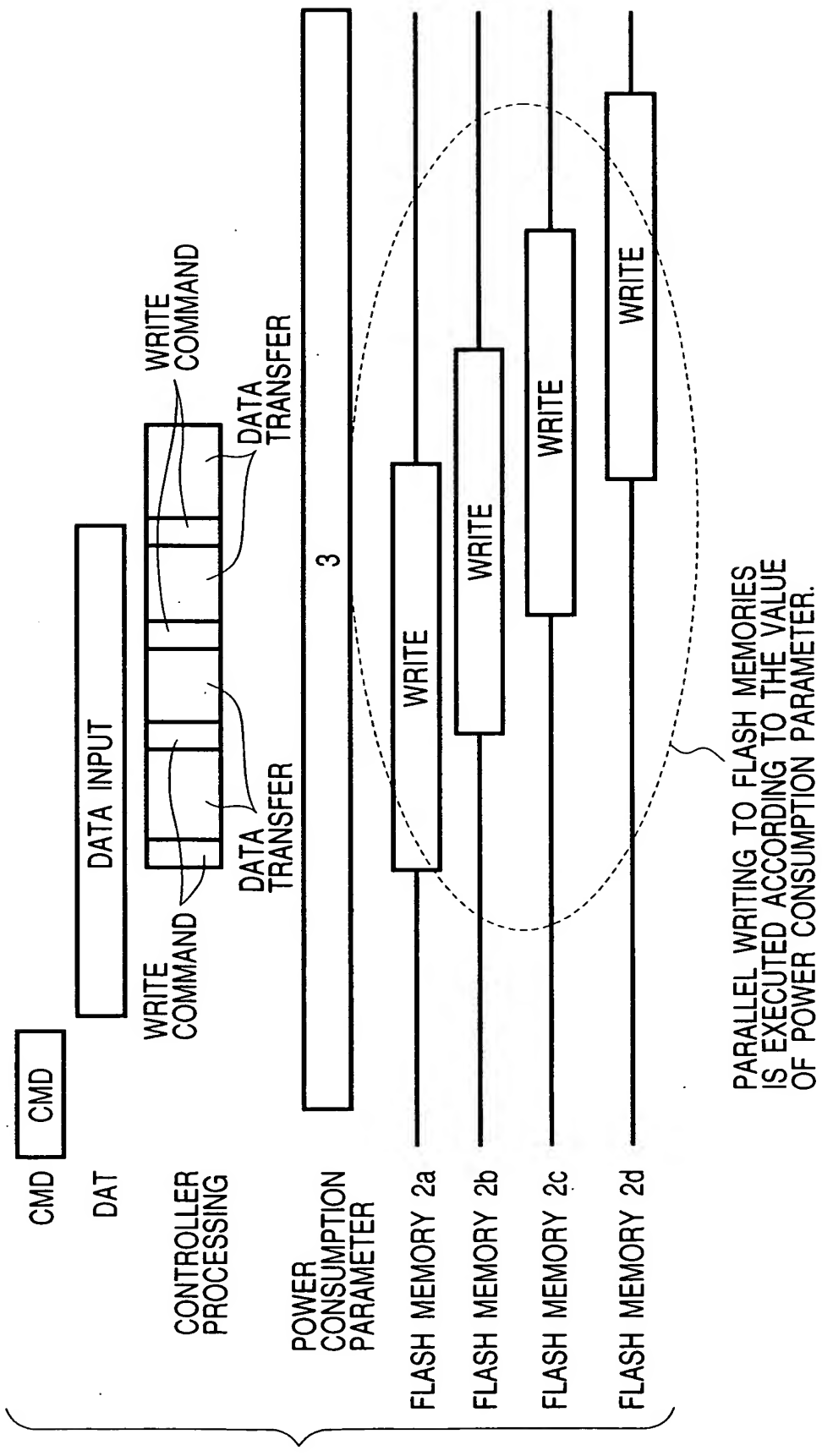

CMD
DAT
CONTROLLER PROCESSING
POWER CONSUMPTION PARAMETER
FLASH MEMORY 2a
FLASH MEMORY 2b
FLASH MEMORY 2c
FLASH MEMORY 2d
CMD
DATA INPUT
WRITE COMMAND
DATA TRANSFER
WRITE COMMAND
DATA TRANSFER
3
WRITE
WRITE
WRITE
WRITE
PARALLEL WRITING TO FLASH MEMORIES IS EXECUTED ACCORDING TO THE VALUE OF POWER CONSUMPTION PARAMETER.

FIG. 19

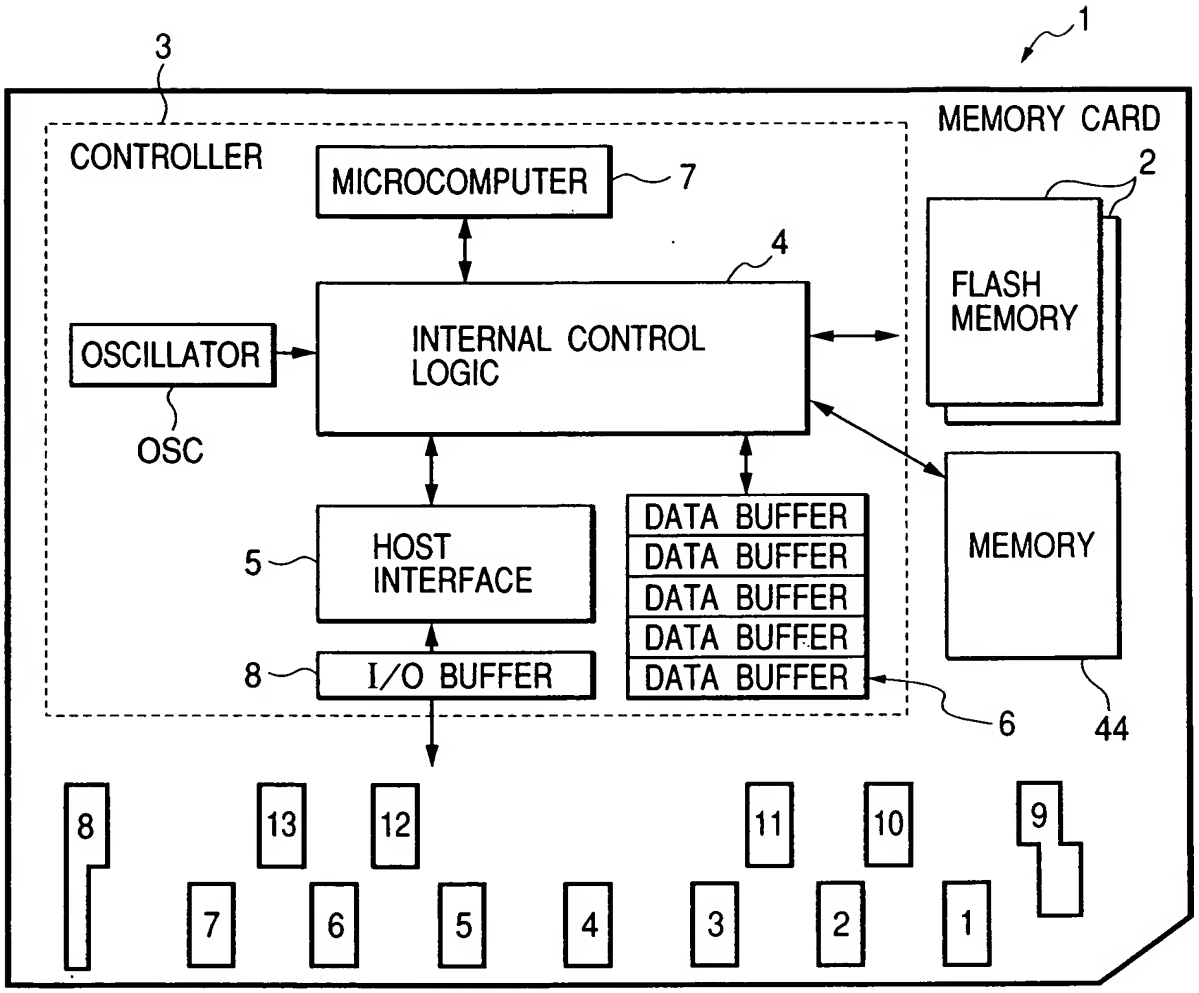

1
3
MEMORY CARD
CONTROLLER
MICROCOMPUTER
7
2
4
FLASH MEMORY
OSCILLATOR
INTERNAL CONTROL LOGIC
OSC
HOST INTERFACE
5
DATA BUFFER
DATA BUFFER
DATA BUFFER
DATA BUFFER
DATA BUFFER
MEMORY
8
I/O BUFFER
6
44
8
13
12
11
10
9
7
6
5
4
3
2
1

FIG. 20

POWER CONSUMPTION PARAMETER REGISTER	TIMING REGISTER = 0			TIMING REGISTER = 1		
	BUS WIDTH × 1	BUS WIDTH × 4	BUS WIDTH × 8	BUS WIDTH × 1	BUS WIDTH × 4	BUS WIDTH × 8
0 (MAX 100mA)	NON-ACTIVATED	NON-ACTIVATED	NON-ACTIVATED	NON-ACTIVATED	NON-ACTIVATED	NON-ACTIVATED
1 (MAX 150mA)	NON-ACTIVATED	NON-ACTIVATED	NON-ACTIVATED	NON-ACTIVATED	NON-ACTIVATED	ACTIVATED
2 (MAX 200mA)	NON-ACTIVATED	NON-ACTIVATED	ACTIVATED	NON-ACTIVATED	ACTIVATED	ACTIVATED
3 (MAX 250mA)	NON-ACTIVATED	ACTIVATED	ACTIVATED	ACTIVATED	ACTIVATED	ACTIVATED

FIG. 21

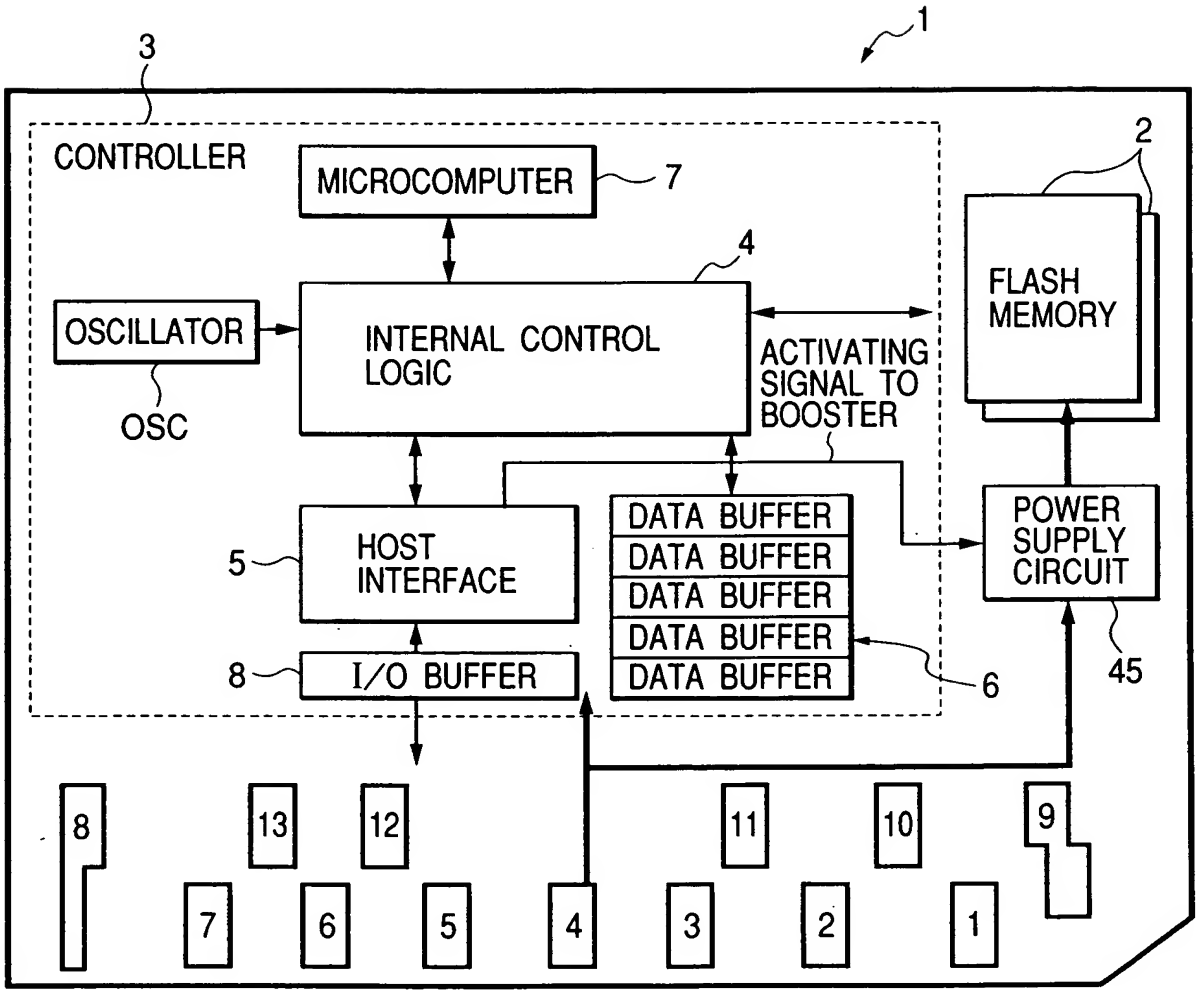

1
3
CONTROLLER
MICROCOMPUTER
7
4
2
FLASH MEMORY
OSCILLATOR
OSC
INTERNAL CONTROL LOGIC
ACTIVATING SIGNAL TO BOOSTER
HOST INTERFACE
5
DATA BUFFER
DATA BUFFER
DATA BUFFER
DATA BUFFER
DATA BUFFER
6
POWER SUPPLY CIRCUIT
45
8
I/O BUFFER
8
13
12
11
10
9
7
6
5
4
3
2
1

FIG. 22

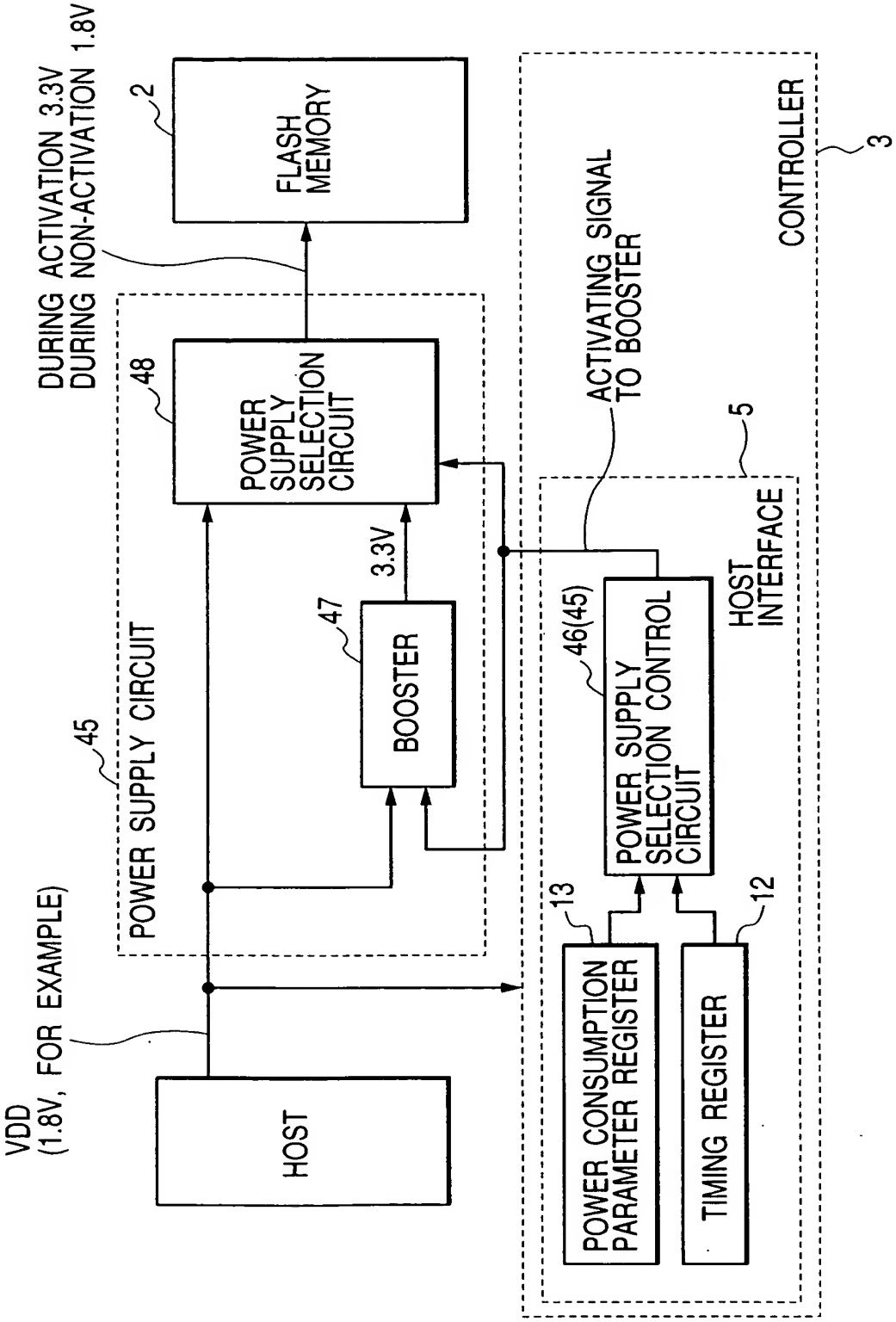

VDD
(1.8V, FOR EXAMPLE)
HOST
DURING ACTIVATION 3.3V
DURING NON-ACTIVATION 1.8V
2
FLASH MEMORY
45
POWER SUPPLY CIRCUIT
48
POWER SUPPLY SELECTION CIRCUIT
47
BOOSTER
3.3V
ACTIVATING SIGNAL TO BOOSTER
CONTROLLER
3
5
HOST INTERFACE
46(45)
POWER SUPPLY SELECTION CONTROL CIRCUIT
13
POWER CONSUMPTION PARAMETER REGISTER
12
TIMING REGISTER

FIG. 23

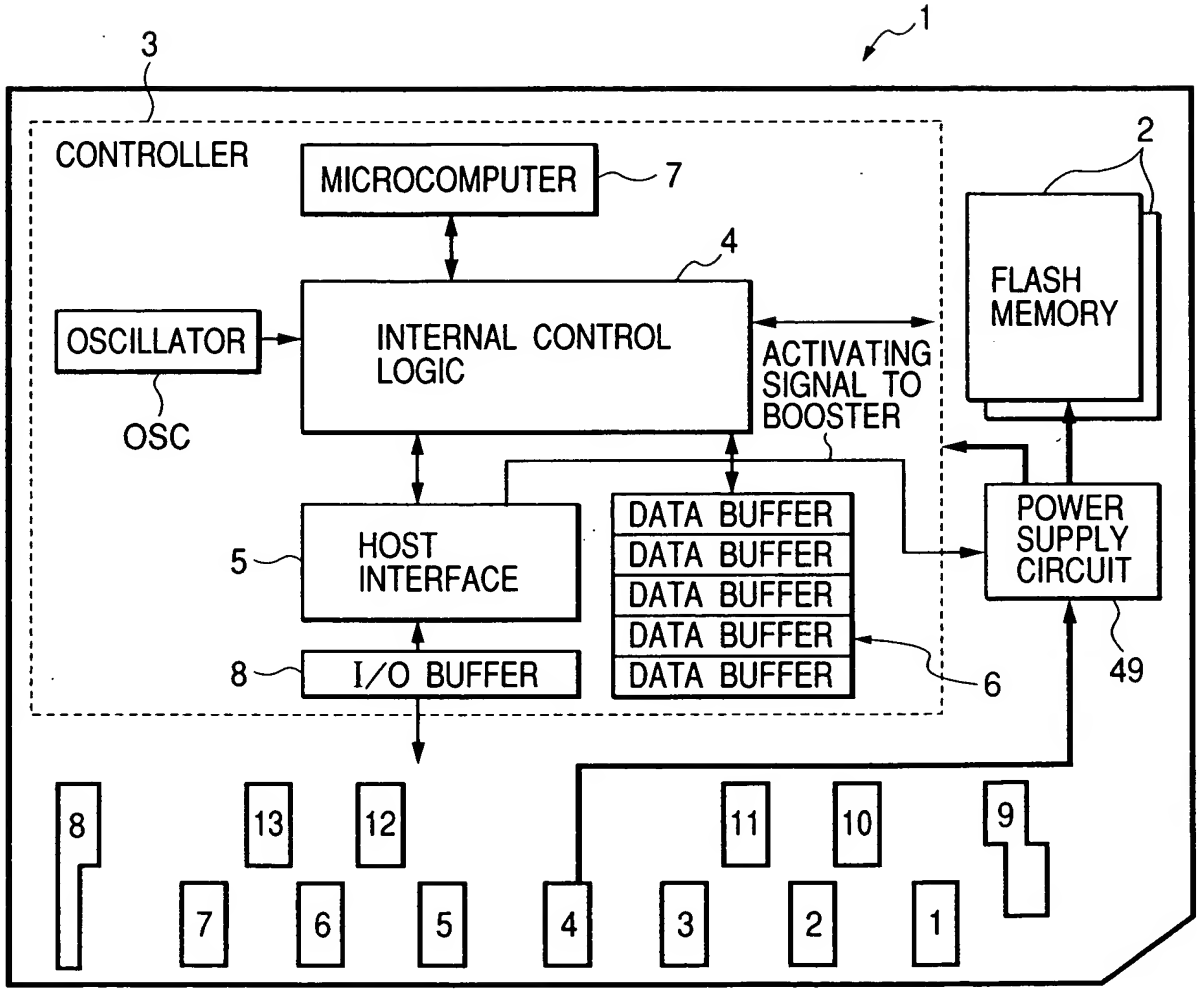

1
3
CONTROLLER
MICROCOMPUTER
7
4
OSCILLATOR
OSC
INTERNAL CONTROL LOGIC
ACTIVATING SIGNAL TO BOOSTER
2
FLASH MEMORY
HOST INTERFACE
5
I/O BUFFER
8
DATA BUFFER
DATA BUFFER
DATA BUFFER
DATA BUFFER
DATA BUFFER
6
POWER SUPPLY CIRCUIT
49
8
13
12
11
10
9
7
6
5
4
3
2
1

FIG. 24

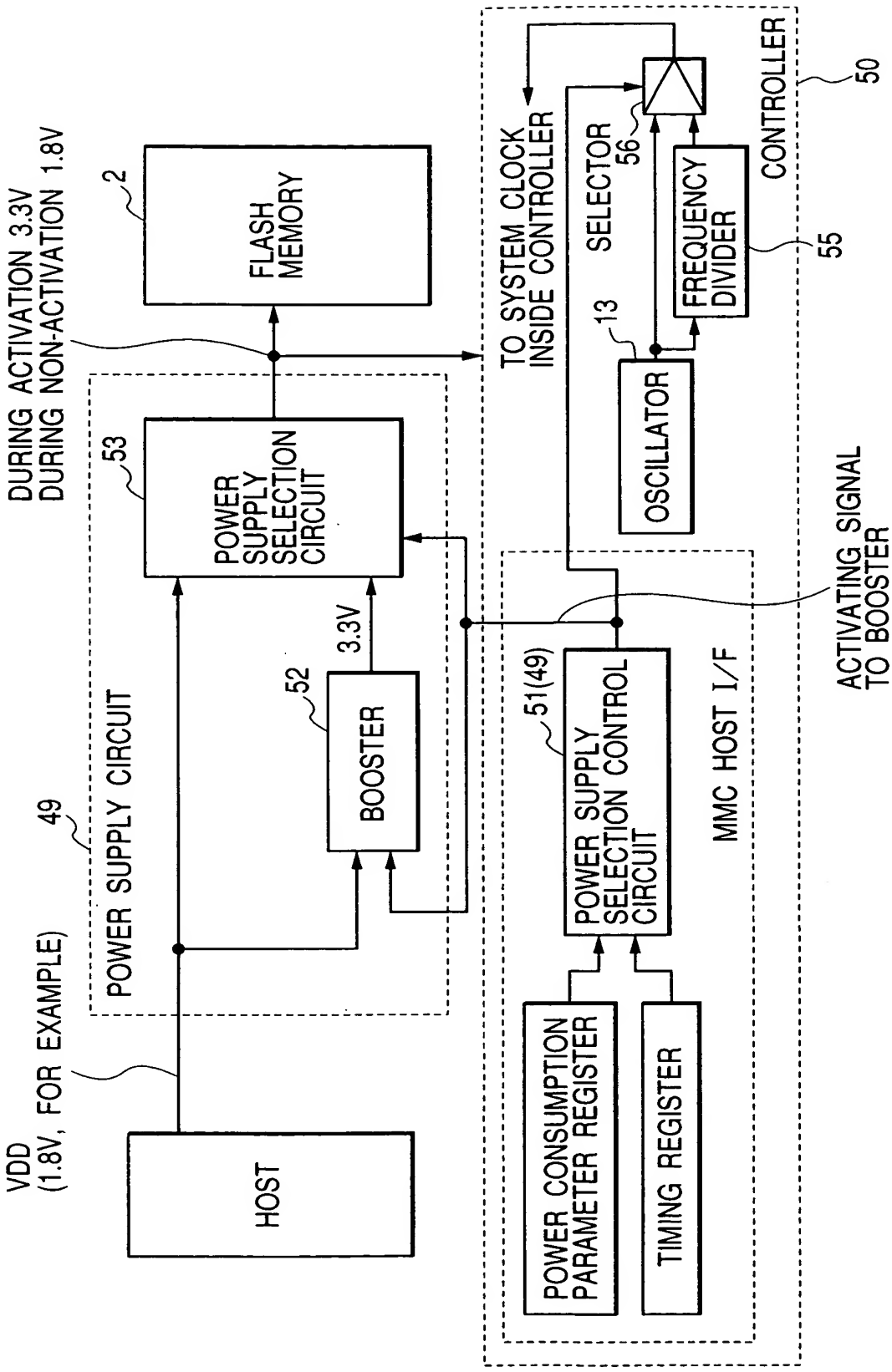

HOST
VDD
(1.8V, FOR EXAMPLE)
POWER SUPPLY CIRCUIT
49
BOOSTER
52
3.3V
POWER SUPPLY SELECTION CIRCUIT
53
DURING ACTIVATION 3.3V
DURING NON-ACTIVATION 1.8V
FLASH MEMORY
2
MMC HOST I/F
POWER SUPPLY SELECTION CONTROL CIRCUIT
51(49)
POWER CONSUMPTION PARAMETER REGISTER
TIMING REGISTER
ACTIVATING SIGNAL TO BOOSTER
OSCILLATOR
13
SELECTOR
56
FREQUENCY DIVIDER
55
CONTROLLER
50
TO SYSTEM CLOCK INSIDE CONTROLLER

FIG. 25

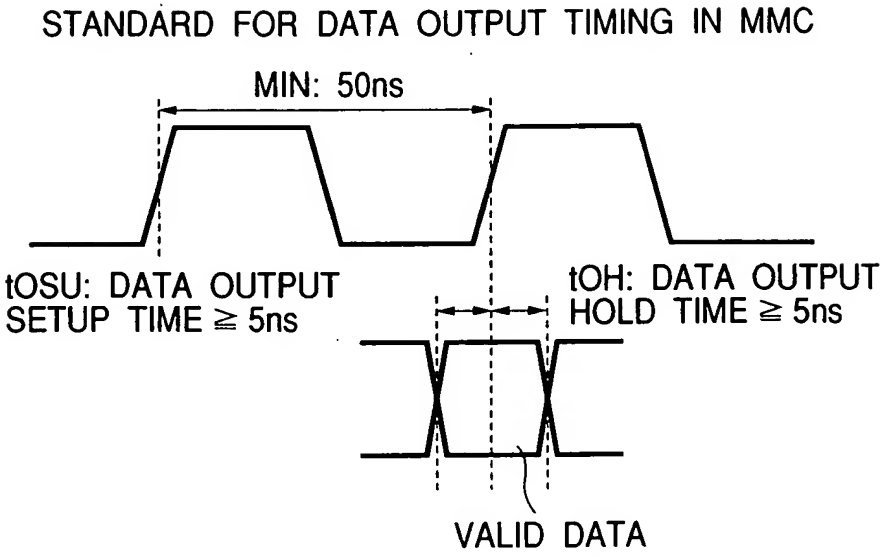

STANDARD FOR DATA OUTPUT TIMING IN MMC
MIN: 50ns
tOSU: DATA OUTPUT
SETUP TIME ≧ 5ns
tOH: DATA OUTPUT
HOLD TIME ≧ 5ns
VALID DATA

FIG. 26

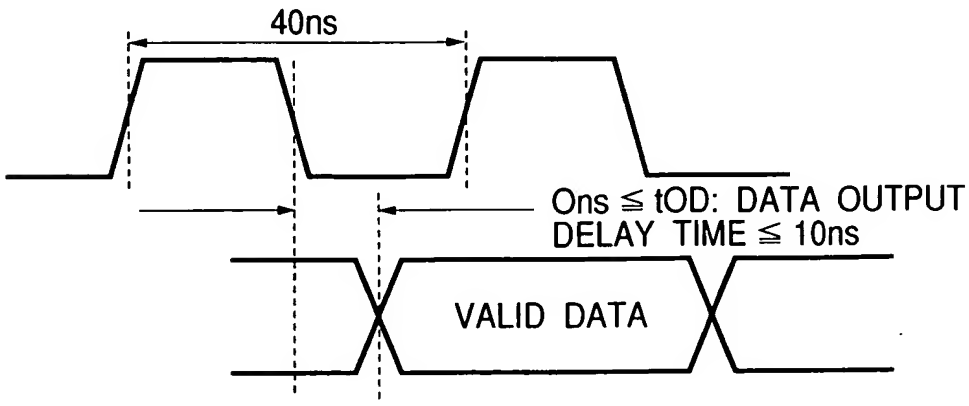
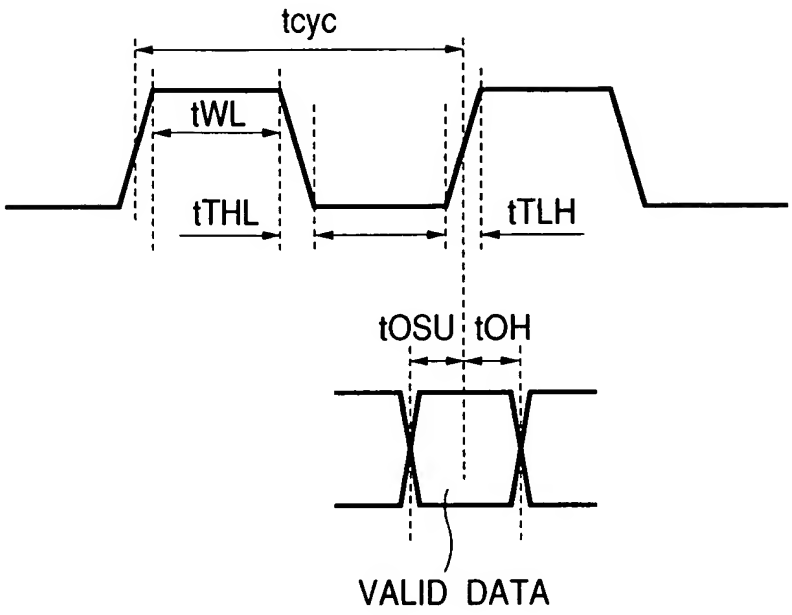

STANDARD FOR DATA OUTPUT TIMING IN SD CARD
40ns
0ns ≦ tOD: DATA OUTPUT
DELAY TIME ≦ 10ns
VALID DATA

FIG. 27



tcyc: CYCLE TIME ≧ 19.2ns
tWL: CLOCK H OR L DURATION ≧ 6.5ns
tTHL: CLOCK FALL TIME ≧ 3ns
tTLH: CLOCK RIZE TIME ≧ 3ns
tOSU: DATA OUTPUT SETUP TIME ≧ 5ns
tOH: DATA OUTPUT HOLD TIME ≧ 5ns